Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.064”**

**.072”**

**VDD**

**HOLDB**

**SCK**

**SI**

**CSB**

**SO**

**WPB**

**GND**

**AT35532**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003”**

**Backside Potential:**

**Mask Ref: AT35532**

**APPROVED BY: DK DIE SIZE .064” X .072” DATE: 9/23/21**

**MFG: ATMEL THICKNESS .011” P/N: AT25640A**

**DG 10.1.2**

#### Rev B, 7/19/02